ISL70003SEH PSPICE Average Model

Introduction

The ISL70003SEH is a radiation and SEE hardened synchronous buck regulator capable of operating over an input voltage range of 3.0V to 13.2V. The ISL70003SEH uses voltage mode control architecture with feed-forward and switches at a selectable frequency of 500kHz or 300kHz. Compensation is externally adjustable to allow for an optimum balance between stability and output dynamic performance. With integrated MOSFETs and class leading radiation performance, this highly efficient single chip power solution is an ideal choice in many space point of load applications.

The PSPICE average model for the ISL700003SEH was developed to help system designers evaluate the operation of this IC prior to or in conjunction with prototyping a system design. This model accurately simulates typical performance characteristics such as loop analysis and transient analysis at room temperature (+25°C). Functionality has been verified on Cadence Orcad 16.6.

Reference Documents

- ISL70003SEH Data Sheet
- ISL70003SEH SMD 5962-14203

License Statement

Project File

The zip folder isl70003seh-pspice-files.zip contains all the necessary files to simulate the average model including the project file (isl70003seh.opj) and the model library (isl70003seh_avg.lib). The application schematic mimics the evaluation board, which is designed for 12V input to 3.3V output conversion, see Figure 1. Three simulation profiles are preset to run an AC loop analysis, start-up and 3A load transient for rapid analysis of the ISL70003SEH, see Figures 4 through 9 for performance curves.

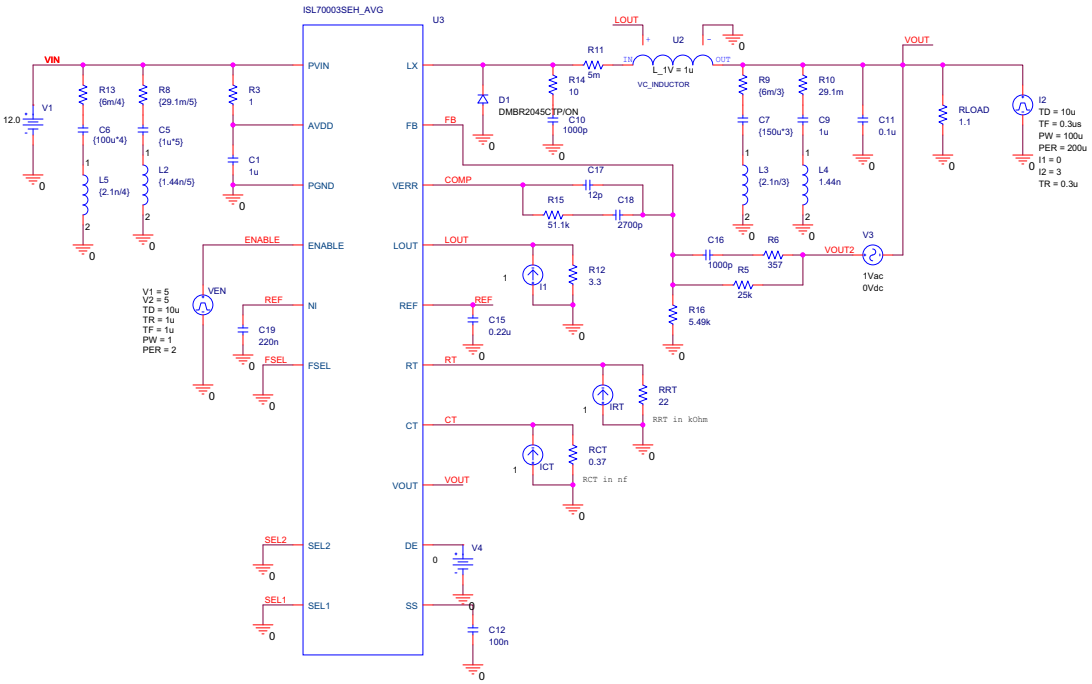

FIGURE 1. ISL70003SEH AVERAGE MODEL APPLICATION SCHEMATIC

Pin Connections

The average model is an equation based model, which needs the operating conditions of the buck regulator in order to properly compute the response of the ISL70003SEH. In order to feed the necessary inputs, the model has been modified to accept the values for LOUT and VOUT.

Inductor - LOUT

The model library, isl70003seh_avg.lib, contains the sub circuit file vc_inductor.subckt. This four terminal inductor must be used to appropriately set the output inductance value used within the model. The IN pin of the inductor must be connected to the LX pin of the ISL70003_AVG model and the OUT pin connects to the output capacitors. A series resistor may be added in line with any of these pins to mimic the DCR of the inductor. The “+” pin should connect the LOUT pin of the ISL70003_AVG model and the “-” pin connects to ground, see Figure 2.

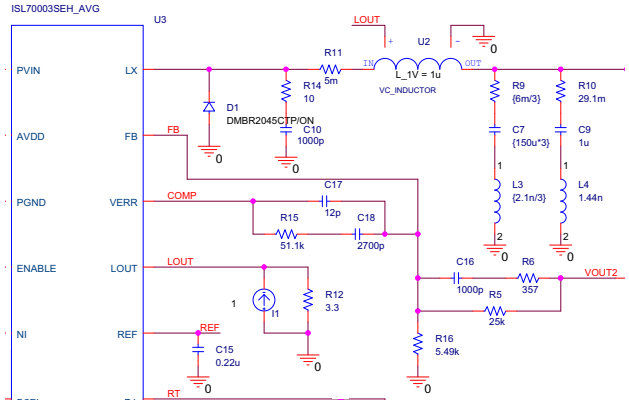

FIGURE 2. VC_INDUCTOR.SUBCKT CONNECTION WITH DCR

To set the output inductor value, a voltage source must be added to the LOUT pin of the ISL70003_AVG model. This voltage is then converted to an inductance value by the equation within the vc_inductor.subckt. The equation is L_1V = 1µ, which translates to 1V is equal to 1µH of inductance. As an example, a 3.3V voltage source connected to the LOUT pin would equal to 3.3µH of the output inductance. In Figure 1, a DC current source and resistor R_{12} are used to create the voltage on the LOUT pin. This allows the user to easily analyze the effects of the inductor’s tolerance by setting R_{12} as a parameter and performing a parametric sweep simulation.

Output Voltage - VOUT

Another pin added to the ISL7003SEH_AVG model is the VOUT pin. This pin is used to sense the output voltage of the regulator and pass the information down into model to compute the operating point. VOUT must be connected to the output voltage of the regulator for the model to work properly.

Sawtooth Ramp - RT/CT

On the ISL70003SEH the RT/CT pin is connected to a resistor and capacitor, which generates the sawtooth ramp that is the input to the comparator that creates the PWM pulse train driving the LX node. In the model, this pin is broken up into two pins (RT and CT) in order to accurately model the feed-forward affect of the regulator. A voltage source is needed at these two pins to set the value for RT and CT. For the RT pin, 1V is equivalent to a resistor of 1kΩ and for the CT pin, 1V is equivalent to a capacitor of 1nF. Figure 3 demonstrates the connection to the RT and CT pins. Note that a current source and resistor are used to generate the voltage on these pins. This allows for easy parametric sweep analysis as PSPICE does not allow tolerances on fixed DC voltage sources.

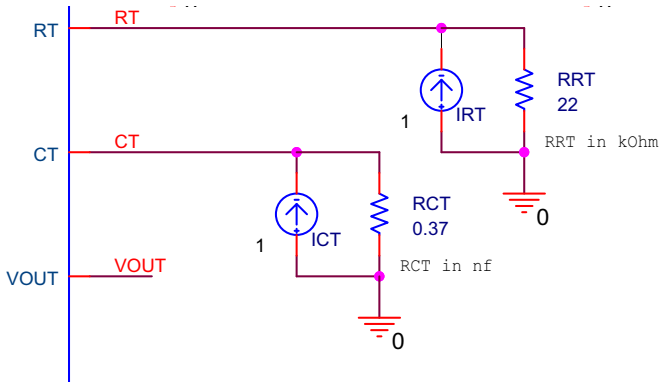

FIGURE 3. RT AND CT PIN CONNECTION

Simulation Performance Curves

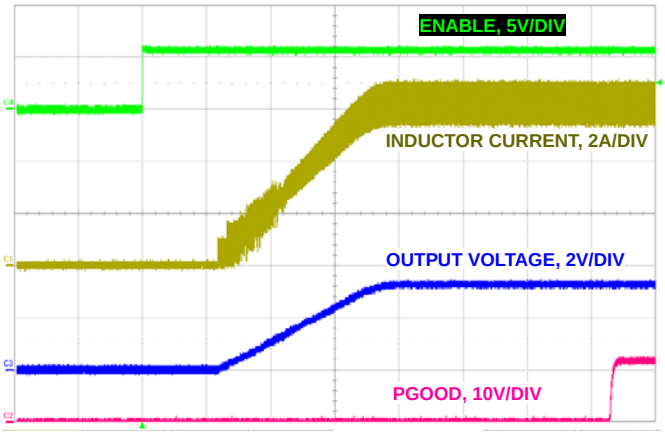

FIGURE 4. CHARACTERIZED SOFT-START WITH 6A LOAD

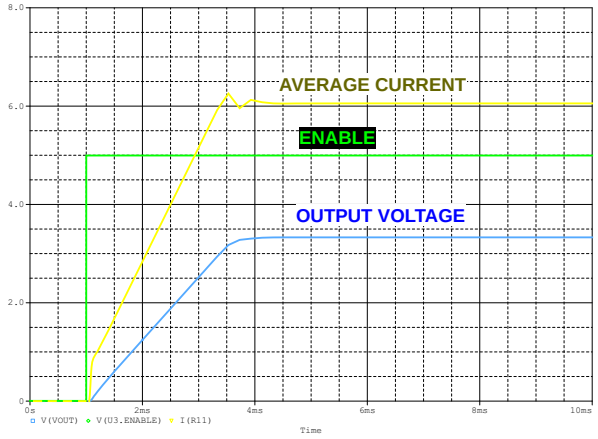

FIGURE 5. SIMULATED SOFT-START WITH 6A LOAD

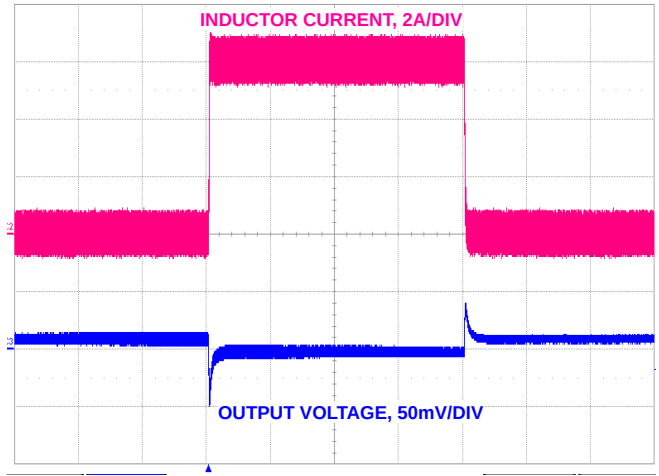

FIGURE 6. CHARACTERIZED 6A LOAD TRANSIENT RESPONSE

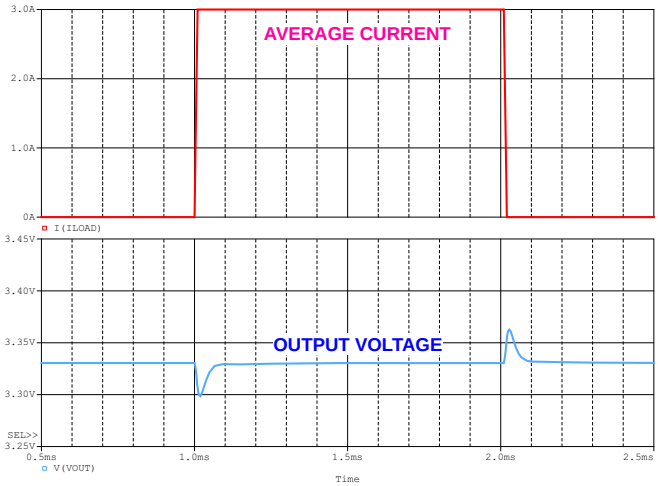

FIGURE 7. SIMULATED 6A LOAD TRANSIENT RESPONSE

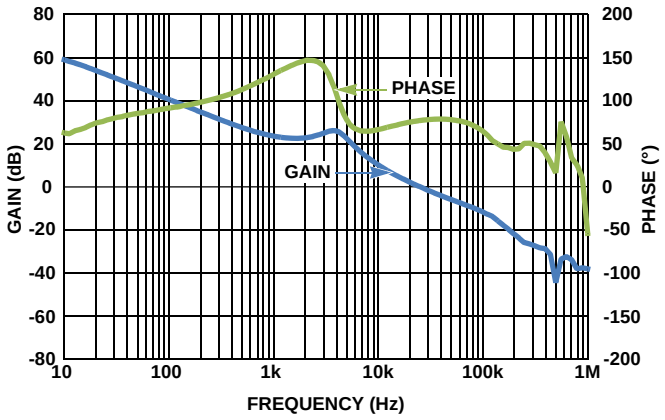

FIGURE 8. CHARACTERIZED LOOP RESPONSE

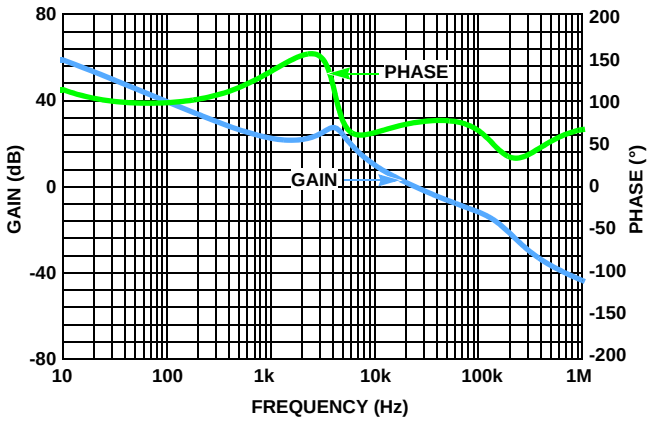

FIGURE 9. SIMULATED LOOP RESPONSE